General Requirements and Information

1

This chapter contains any requirements which apply to all devices contained in this document.

1.1 General Requirements

Requirements:

1–1. The interfaces define in this document must not be accessed by RTAS or marked as *used-by-rtas* with two exception as follows:

a. Any RTAS service that does not return to the operating system may access any interface.

b. The interfaces in Chapter 13, “Graphics,” on page 161 may be accessed by the RTAS *display-character* function, if the graphics interface in the Open Firmware device tree node does not contain the *used-by-rtas* property, but is the device indicated by the *rtas-display-device* property.

1–2. If the implementation of the devices in this document have additional registers which are not part of the programming model given in this document, then these registers must not be required for correct operation of the device by the operating system and they must all be declared in the Open Firmware device tree to prevent other devices from being assigned to their addresses.

1–3. Any controller not contained on standard adaptor cards for their I/O bus must have the *builtin* property.

1.2 Credit for Material

Some material in this specification has been copied from documentation describing existing components. Credit for this material is given in the following section.

1.2.1 From National Semiconductor Corporation

Material in some chapters was copied from *National Semiconductor PC87308VUL SuperI/O*^{TM} *Enhanced Sidewinder Lite Plug and Play Compatible Chip, with a Floppy Disk Controller, a Keyboard Controller, a Real-Time Clock, Two UARTs, Full Infrared Support and an IEEE1284 Parallel Port* [24]. and was reprinted with permission of National Semiconductor Corporation.

National Semiconductor asked that the following Life Support Policy be included.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ISA DMA Controller

2

2.1 Minimum System Requirements

The Direct Memory Access (DMA) controller allows I/O devices to transfer data directly to and from memory. The minimum system requirements are shown in Table 1 on page 3, which is an excerpt from *PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture* [1].

Table 1. Summary of Minimum Requirements for ISA DMA (excerpt)

Subsystem	Specification	Portable	Personal	Server	Description
Direct Memory Access (DMA)	ISA	R	R	R	[20] ISA DMA must be 82378ZB compatible.

Logically, the DMA Controller is actually two controllers designated DMA Controller 1 and DMA Controller 2 as shown in Figure 1 on page 3. When DMA Controller 1 is controlling DMA transfers, channels 0-3 are capable of 8 bit count by byte transfers. When DMA Controller 2 is controlling DMA transfers, channels 5-7 are capable of 16 bit count by word (2 byte) transfers. (ISA bus masters are not affected by those restrictions.) Channel 4 is used for cascading DMA Controller 1 to DMA Controller 2 and is unusable for data transfer with an ISA slave device.

There are two modes of operation for the DMA transfers: Scatter/Gather mode and DMA mode. In DMA mode, all the control information necessary for the DMA controller to make a transfer is programmed into the DMA controller's registers. This means that a single buffer can be transferred on a given DMA channel before host processor service is required. In Scatter/Gather mode (abbreviated S/G mode), software builds a list of Scatter/Gather Descriptors (SGD's) in system memory and provides a pointer to the DMA controller that gives the start of the list. Software then issues commands to start and stop the processing of the SGD list by the DMA controller.

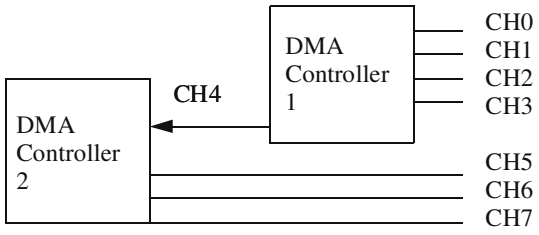


Figure 1. Cascaded DMA Controllers

Requirements:

2–1. An ISA DMA Controller must be compatible with the Intel 82378ZB System I/O (SIO), except as noted in the following requirements in this chapter.

2–2. This device (ISA DMA Controller) must be addressed only with ISA I/O addresses.

2.2 References

3. *Intel 82378ZB System I/O (SIO) Specification* [20]
4. *SL82C565 System I/O Controller With PCI Arbiter*, from Winbond Systems Laboratory [21]
5. *CHRP ISA DMA Controller Device Binding to IEEE 1275-1994 Standard for Boot (Initialization, Configuration) Firmware* [22]

2.3 ISA DMA Controller Open Firmware Properties

Requirements:

2–3. This device must be represented by the Open Firmware properties “name=dma-controller, device_type=dma-controller, compatible= chrp,dma”.

2–4. This device must have the Open Firmware properties defined in *CHRP ISA DMA Controller Device Binding to: IEEE 1275-1994 Standard for Boot (Initialization, Configuration) Firmware*.

2–5. The registers shown in Table 2 on page 5, Register Map for ISA DMA Device, must all be present in the device defined in this chapter.

2–6. All the reg property fields specified in Table 2 on page 5 must comply with the format given in the *ISA Bus Binding to: IEEE 1275-1994 Standard for Boot (Initialization, Configuration) Firmware*.

2–7. This device must be represented as an ISA device and a child of an ISA bridge node in the Open Firmware device tree.

The positions in the reg property (denoted by reg[1], reg[2], etc.) and the value of the size fields are stated in Table 2 on page 5. The format is described in the referenced Open Firmware bindings and not repeated in this document.

The ISA DMA Controller register map and Reg properties are shown below in Table 2 on page 5.

Table 2. Register Map for ISA DMA Device

Offset	Traditional ISA I/O Address	Register		Reg Property
		Read	Write	
0x00	0x0000	Ch0 Current Addr Reg (CA0)	Ch0 Current Addr Reg (CA0)	
			Ch0 Base Addr Reg (BA0)	
0x01	0x0001	Ch0 Current Cnt Reg (CC0)	Ch0 Current Cnt Reg (CC0)	
			Ch0 Base Cnt Reg (BC0)	
0x02	0x0002	Ch1 Current Addr Reg (CA1)	Ch1 Current Addr Reg (CA1)	
			Ch1 Base Addr Reg (BA1)	
0x03	0x0003	Ch1 Current Cnt Reg (CC1)	Ch1 Current Cnt Reg (CC1)	
			Ch1 Base Cnt Reg (BC1)	
0x04	0x0004	Ch2 Current Addr Reg (CA2)	Ch2 Current Addr Reg (CA2)	
			Ch2 Base Addr Reg (BA2)	
0x05	0x0005	Ch2 Current Cnt Reg (CC2)	Ch2 Current Cnt Reg (CC2)	
			Ch2 Base Cnt Reg (BC2)	
0x06	0x0006	Ch3 Current Addr Reg (CA3)	Ch3 Current Addr Reg (CA3)	
			Ch3 Base Addr Reg (BA3)	
0x07	0x0007	Ch3 Current Cnt Reg (CC3)	Ch3 Current Cnt Reg (CC3)	
			Ch3 Base Cnt Reg (BC3)	
0x08	0x0008	DMA 1 Status Register (DS1)	DMA 1 Command Register (DCOM1)	reg[1],Size=16 bytes
0x09	0x0009		DMA 1 Request Register (DR1)	
0x0A	0x000A		DMA 1 Write Single Bit Mask Register (WSM1)	
0x0B	0x000B		DMA 1 Channel Mode Register (DCM1)	
0x0C	0x000C		DMA 1 Clear Byte Pointer Register (CBP1)	
0x0D	0x000D		DMA 1 Master Clear (DMC1)	
0x0E	0x000E		DMA 1 Clear Mask Register (DCLM1)	
0x0F	0x000F		DMA 1 Write All Mask Register (WAM1)	
0x00	0x0080	Reserved		
0x01	0x0081	CH2 Current Low Page Register (CLOP2	CH2 Current Low Page Register (CLOP2)	
			CH2 Base Low Page Register (BLOP2)	
0x02	0x0082	CH3 Current Low Page Register (CLOP3)	CH3 Current Low Page Register (CLOP3)	
			CH3 Base Low Page Register (BLOP3)	
0x03	0x0083	CH1 Current Low Page Register (CLOP1)	CH1 Current Low Page Register (CLOP1)	
			CH1 Base Low Page Register (BLOP1)	

Table 2. Register Map for ISA DMA Device ***(Continued)***

Offset	Traditional ISA I/O Address	Register		Reg Property
		Read	Write	
0x04	0x0084	Reserved		
0x05	0x0085	Reserved		reg[2],Size=16 bytes
0x06	0x0086	Reserved		
0x07	0x0087	CH0 Current Low Page Register (CLOP0)	CH0 Current Low Page Register (CLOP0)	
			CH0 Base Low Page Register (BLOP0)	
0x08	0x0088	Reserved		
0x09	0x0089	CH6 Current Low Page Register (CLOP6)	CH6 Current Low Page Register (CLOP6)	
			CH6 Base Low Page Register (BLOP6)	
0x0A	0x008A	CH7 Current Low Page Register (CLOP7)	CH7 Current Low Page Register (CLOP7)	
			CH7 Base Low Page Register (BLOP7)	
0x0B	0x008B	CH5 Current Low Page Register (CLOP5)	CH5 Current Low Page Register (CLOP5)	
			CH5 Base Low Page Register (BLOP5)	
0x0C-0x0E	0x008C-0x008E	Reserved		
0x0F	0x008F	Reserved		
0x00	0x00C0	Reserved		
0x01	0x00C1	Reserved		
0x02	0x00C2	Reserved		
0x03	0x00C3	Reserved		
0x04	0x00C4	Ch5 Current Addr Reg (CA5)	Ch5 Current Addr Reg (CA5)	
			Ch5 Base Addr Reg (BA5)	
0x05	0x00C5	Reserved		
0x06	0x00C6	Ch5 Current Cnt Reg (CC5)	Ch5 Current Cnt Reg (CC5)	
			Ch5 Base Cnt Reg (BC5)	
0x07	0x00C7	Reserved		
0x08	0x00C8	Ch6 Current Addr Reg (CA6)	Ch6 Current Addr Reg (CA6)	
			Ch6 Base Addr Reg (BA6)	
0x09	0x00C9	Reserved		
0x0A	0x00CA	Ch6 Current Cnt Reg (CC6)	Ch6 Current Cnt Reg (CC6)	
			Ch6 Base Cnt Reg (BC6)	
0x0B	0x00CB	Reserved		reg[3], Size=32 bytes
0x0C	0x00CC	Ch7 Current Addr Reg (CA7)	Ch7 Current Addr Reg (CA7)	
			Ch7 Base Addr Reg (BA7)	
0x0D	0x00CD	Reserved		

Table 2. Register Map for ISA DMA Device ***(Continued)***

Offset	Traditional ISA I/O Address	Register		Reg Property
		Read	Write	
0x0E	0x00CE	Ch7 Current Cnt Reg (CC7)	Ch7 Current Cnt Reg (CC7)	
			Ch7 Base Cnt Reg (BC7)	
0x0F	0x00CF	Reserved		
0x10	0x00D0	DMA 2 Status Register (DS2)	DMA 2 Command Register (DCOM2)	
0x11	0x00D1	Reserved		
0x12	0x00D2		DMA 2 Request Reg (DR2)	
0x13	0x00D3	Reserved		
0x14	0x00D4		DMA 2 Write Single Bit Mask Register (WSM2)	
0x15	0x00D5	Reserved		
0x16	0x00D6		DMA 2 Channel Mode Register (DCM2)	
0x17	0x00D7	Reserved		
0x18	0x00D8		DMA 2 Clear Byte Pointer Reg (CBP2)	
0x19	0x00D9	Reserved		
0x1A	0x00DA		DMA 2 Master Clear Register (DMC2)	
0x1B	0x00DB	Reserved		
0x1C	0x00DC		DMA 2 Clear Mask (DCLM2)	
0x1D	0x00DD	Reserved		
0x1E	0x00DE		DMA 2 Write All Mask (WAM2)	
0x1F	0x00DF	Reserved		
0x00	0x040A	Scatter/Gather Interrupt Status Register (SGIS)		reg[4], Size=1 byte
0x00	0x040B		DMA 1 Extended Mode Register (DCEM1)	reg[5], Size=1 byte
0x00	0x0410		CH0 Scatter/Gather Command (SGC0)	
0x01	0x0411		CH1 Scatter/Gather Command (SGC1)	
0x02	0x0412		CH2 Scatter/Gather Command (SGC2)	
0x03	0x0413		CH3 Scatter/Gather Command (SGC3)	
0x04	0x0414	Reserved		
0x05	0x0415		CH5 Scatter/Gather Command (SGC5)	
0x06	0x0416		CH6 Scatter/Gather Command (SGC6)	
0x07	0x0417		CH7 Scatter/Gather Command (SGC7)	
0x08	0x0418	CH0 Scatter/Gather Status (SGS0)		

Table 2. Register Map for ISA DMA Device ***(Continued)***

Offset	Traditional ISA I/O Address	Register		Reg Property
		Read	Write	
0x09	0x0419	CH1 Scatter/Gather Status (SGS1)		reg[6], Size=48 bytes
0x0A	0x041A	CH2 Scatter/Gather Status (SGS2)		
0x0B	0x041B	CH3 Scatter/Gather Status (SGS3)		
0x0C	0x041C	Reserved		
0x0D	0x041D	CH5 Scatter/Gather Status (SGS5)		
0x0E	0x041E	CH6 Scatter/Gather Status (SGS6)		
0x0F	0x041F	CH7 Scatter/Gather Status (SGS7)		
0x10-0x13	0x0420-0x0423	CH0 Scatter/Gather Descriptor Table Pointer (SGPTR0)		
0x14-0x17	0x0424-0x0427	CH1 Scatter/Gather Descriptor Table Pointer (SGPTR1)		
0x18-0x1B	0x0428-0x042B	CH2 Scatter/Gather Descriptor Table Pointer (SGPTR2)		
0x1C-0x1F	0x042C-0x042F	CH3 Scatter/Gather Descriptor Table Pointer (SGPTR3		
0x20-0x23	0x0430-0x0433	Reserved		
0x24-0x27	0x0434-0x0437	CH5 Scatter/Gather Descriptor Table Pointer (SGPTR5)		
0x28-0x2B	0x0438-0x043B	CH6 Scatter/Gather Descriptor Table Pointer (SGPTR6)		
0x2C-0x2F	0x043C-0x043F	CH7 Scatter/Gather Descriptor Table Pointer (SGPTR7)		
0x00	0x481	CH 2 Current High Page Register (CHIP2)	CH 2 Current High Page Register (CHIP2)	reg[7], Size=11 bytes
			CH 2 Base High Page Register (BHIP2)	
0x01	0x482	CH 3 Current High Page Register (CHIP3)	CH 3 Current High Page Register (CHIP3)	
			CH 3 Base High Page Register (BHIP3)	
0x02	0x483	CH 1Current High Page Register (CHIP1)	CH 1 Current High Page Register (CHIP1)	
			CH 1 Base High Page Register (BHIP1)	
0x03-0x05	0x484-0x486	Reserved		
0x06	0x487	CH 0 Current High Page Register (CHIP0)	CH 0 Current High Page Register (CHIP0)	
			CH 0 Base High Page Register (BHIP0)	
0x07	0x488	Reserved		

Table 2. Register Map for ISA DMA Device ***(Continued)***

Offset	Traditional ISA I/O Address	Register		Reg Property
		Read	Write	
0x08	0x489	CH 6 Current High Page Register (CHIP6)	CH 6 Current High Page Register (CHIP6)	
			CH 6 Base High Page Register (BHIP6)	
0x09	0x48A	CH 7 Current High Page Register (CHIP7)	CH 7 Current High Page Register (CHIP7)	
			CH 7 Base High Page Register (BHIP7)	
0x0A	0x48B	CH 5 Current High Page Register (CHIP5)	CH 5 Current High Page Register (CHIP5)	
			CH 5 Base High Page Register (BHIP5)	
0x00	0x4D6		DMA 2 Extended Mode Register (DCEM2)	reg[8], Size=1 byte

2.4 DMA Channel Registers

2.4.1 Current Address Register 0 (CA0)

Table 3. Current Address Register 0 (CA0) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
2 byte	Indirect	reg[1]	0x00	Read/Write	undefined	N/A

DMA Channel 0 has a 16 bit Base Address Register, BA0, and a 16 bit Current Address Register, CA0. The CA0 is described here. CA0 contains the address the DMA channel is currently using. It is used for both scatter/gather and DMA operations. Before writing to this register, the DMA Clear Byte Pointer Register (Section 2.5.15, “DMA 1 Clear Byte Pointer Register (CBP1),” on page 23) must be written to reset an internal flip flop that prepares this 16 bit register for two successive byte writes. CA0 and BA0 are located at the same address. CA0 is incremented or decremented with each transfer depending on the DMA channel 0 mode settings. BA0 stores the initial value of CA0 (Section 2.4.3, “Base Address Register 0 (BA0),” on page 10). CA0 is autoinitialized back to its starting value after a terminal count, TC, if autoinitialize mode is set in the DMA Channel Mode Register 1 (Section 2.5.3, “DMA 1 Channel Mode Register (DCM1),” on page 16.)

Table 4. Current Address Register (CA0)

Bit	Function
15 -8	**High order address byte**: This is the second byte written after a DMA Clear Byte Pointer command.
7-0	**Low order address byte**: This is the first byte written after a DMA Clear Byte Pointer command

2.4.2 Current Address Registers (CA1-CA7)

Current Address Registers 1-7, CA1-CA7, are identical to Current Address Register 0 (Section 2.4.1, “Current Address Register 0 (CA0),” on page 9) with the following exceptions:

1. they are associated with the other DMA channels as indicated by their numeric suffix (i.e. CA5 is the Current Address Register for DMA channel 5). They have unique addresses as shown in Table 2 on page 5
2. The address programmed into CA5-CA7 must be an even address that has been shifted right by one bit. The High Page register (Section 2.4.13, “Current High Page Register 0 (CHIP0),” on page 13) and Low Page register (Section 2.4.9, “Current Low Page Register 0 (CLOP0),” on page 12) are not shifted by software. As an example, for address 0x1FE, the address programmed into the Current Address register is 0xFF.

2.4.3 Base Address Register 0 (BA0)

Table 5. Base Address Register 0 (BA0) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
2 byte	Indirect	reg[1]	0x00	Write Only	undefined	N/A

DMA Channel 0 has a 16-bit Base Address Register, BA0, which stores the initial value of CA0 for DMA operations. Before writing to this register, the DMA Clear Byte Pointer Register must be written to reset an internal flip flop that prepares this 16 bit register for two successive byte writes (Section 2.5.15, “DMA 1 Clear Byte Pointer Register (CBP1),” on page 23). CA0 and BA0 are located at the same address. For DMA operations, BA0 is used to reload the starting value for CA0 after a terminal count, TC, if autoinitialize mode is set in the DMA Channel Mode Register 1 (Section 2.5.3, “DMA 1 Channel Mode Register (DCM1),” on page 16). During scatter/gather operations, the DMA controller loads a reserve buffer into BA0.

Table 6. Base Address Register (BA0)

Bit	Function
15 -8	**High order address byte**: this is the second byte written after a DMA Clear Byte Pointer command.
7-0	**Low order address byte**: This is the first byte written after a DMA Clear Byte Pointer command

2.4.4 Base Address Registers 1-7 (BA1-BA7)

Base Address Registers 1-7, BA1-BA7, are identical to Base Address Register 0 (Section 2.4.3, “Base Address Register 0 (BA0),” on page 10) with the following exceptions:

1. they are associated with the other DMA channels as indicated by their numeric suffix (i.e. BA5 is the Base Address Register for DMA channel 5). They have unique addresses as shown in Table 2 on page 5
2. The address programmed into BA5-BA7 must be an even address that has been shifted right by one bit. The High Page register (1.3.13 on page 12) and Low Page register (1.3.9 on page 11) are not shifted by software. As an example, for address 0x1FE, the address programmed into the Base Address register is 0xFF.

2.4.5 Current Count Register 0 (CC0)

Table 7. Current Count Register 0 (CC0) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
2 byte	Indirect	reg[1]	0x01	Read/Write	undefined	N/A

DMA Channel 0 has a 16 bit Current Count Register, CC0, and a 16 bit Base Count Register 0, BC0. CC0 is described here. It contains the “number of bytes to be transferred - 1”. It is used for both scatter/gather and DMA operations. Before writing to this register, the DMA Clear Byte Pointer Register must be written to reset an internal flip flop that prepares this 16 bit register for two successive byte writes (Section 2.5.15, “DMA 1 Clear Byte Pointer Register (CBP1),” on page 23). CC0 and BC0 are located at the same address. CC0 is decremented with each transfer. BC0 is write only and stores the initial value of CC0 (Section 2.4.7, “Base Count Register 0 (BC0),” on page 12). When CC0 goes from 0x0000 to 0xFFFF a terminal count, TC, is generated. If autoinitialize mode is set in the DMA Channel Mode Register 1 (Section 2.5.3, “DMA 1 Channel Mode Register (DCM1),” on page 16) CC0 is autoinitialized to Base Count Register 0 (Section 2.4.7, “Base Count Register 0 (BC0),” on page 12) after a TC. During scatter/gather mode operations, CC0 contains the 16 bits of the current byte count.

Table 8. Current Count Register (CC0)

Bit	Function
15 -8	**High order byte**
7-0	**Low order byte**

2.4.6 Current Count Registers 1-7 (CC1-CC7)

Current Count Registers 1-7, CC1-CC7, are identical to Current Count Register 0 (Section 2.4.5, “Current Count Register 0 (CC0),” on page 11) with the following exceptions:

1. they are associated with the other DMA channels as indicated by their numeric suffix (i.e. CC5 is the Current Count Register for DMA channel 5). They have unique addresses shown in Table 2 on page 5
2. CC1 through CC3 initially contain the number of bytes to be transferred -1, and decrement with each byte transferred. Note: some hardware designs may allow CC1 through CC3 to count word (16-bit) transfers. The architecture only requires them to count byte transfers.
3. CC5 through CC7 initially contain the number of words (16 bits) to be transferred - 1, and decrement with each word transferred. Note: some hardware designs may allow CC5 through CC7 to count byte transfers. The architecture only requires them to count word transfers.
4. DMA Channel Mode Register 2 controls autoinitialize for channels 5-7.

2.4.7 Base Count Register 0 (BC0)

Table 9. Base Count Register (BC0) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
2 byte	Indirect	reg[1]	0x01	Write Only	undefined	N/A

DMA Channel 0 has a 16 bit Base Count Register 0, BC0. The “number of bytes to be transferred-1” is programmed into BC0. It is used for both DMA and scatter/gather operations. Before writing to this register, the DMA Clear Byte Pointer Register (Section 2.5.15, “DMA 1 Clear Byte Pointer Register (CBP1),” on page 23) must be written to reset an internal flip flop that prepares this 16 bit register for two successive byte writes. CC0 and BC0 are located at the same address. BC0 is write only and stores the initial value of CC0 (Section 2.4.5, “Current Count Register 0 (CC0),” on page 11). In scatter/gather mode, BC0 is used to store a reserve buffer.

Table 10. Base Count Register (BC0)

Bit	Function
15 -8	**High order byte**
7-0	**Low order byte**

2.4.8 Base Count Registers 1-7 (BC1-BC7)

Base Count Registers 1-7, BC1-BC7, are identical to Base Count Register 0 (Section 2.4.7, “Base Count Register 0 (BC0),” on page 12) with the following exceptions:

1. they are associated with the other DMA channels as indicated by their numeric suffix (i.e. BC5 is the Base Count Register for DMA channel 5). They have unique addresses shown in Table 2 on page 5.
2. BC1 through BC3 contain the number of bytes to be transferred-1. Note: some hardware designs may allow BC1-BC3 to contain the number of words (16 bits) to be transferred. The architecture only requires them to handle bytes.
3. BC5 through BC7 contain the number of words to be transferred. Note: some hardware designs may allow BC5-BC7 to contain the number of bytes to be transferred. The architecture only requires them to handle words.

2.4.9 Current Low Page Register 0 (CLOP0)

Table 11. Current Low Page Register 0 (CLOP0) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[2]	0x07	Read/Write	undefined	N/A

Each DMA channel has a Current Low Page Register, Base Low Page Register, Current High Page Register and Base High Page Register. The Current Low Page Register 0, CLOP0, provides the second most significant byte, bits 23-16, of the 32 bit current address for both DMA and Scatter/Gather (S/G) transfers on DMA channel 0. If the Current Address Register 0, CA0, overflows or underflows during a S/G transfer, the CLOP0 register must be incremented or decremented accordingly. CLOP0 need not increment/decrement during a DMA operation, although some hardware designs may allow it. The Current Low Page Register, CLOP0, and the Base Low Page Register, BLOP0 (Section 2.4.11, "Base Low Page Register 0 (BLOP0)," on page 13), are at the same address and are written concurrently.

2.4.10 Current Low Page Register 1-7 (CLOP1-CLOP7)

Current Low Page Registers 1-7, CLOP1-CLOP7, are identical to Current Low Page Register 0 (Section 2.4.9, "Current Low Page Register 0 (CLOP0)," on page 12) with the exception they are associated with the other DMA channels as indicated by their numeric suffix (i.e. CLOP5 is the Current Low Page Register for DMA channel 5). They have unique addresses as shown in Table 2 on page 5.

2.4.11 Base Low Page Register 0 (BLOP0)

Table 12. Base Low Page Register 0 (BLOP0) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[2]	0x07	Write Only	undefined	N/A

Each DMA channel has a Base Low Page Register which holds the initial value programmed into its Current Low Page Register. Base Low Page Register 0, BLOP0, is the Base Low Page Register for channel 0. If autoinitialize is enabled in the DMA Channel Mode register (Section 2.5.3, "DMA 1 Channel Mode Register (DCM1)," on page 16), BLOP0 is copied into CLOP0 after a Terminal Count (TC). During a scatter/gather operation, BLOP0 is used to hold a reserve buffer.

2.4.12 Base Low Page Register 1-7 (BLOP1-BLOP7)

Base Low Page Registers 1-7, BLOP1-BLOP7, are identical to Base Low Page Register 0 (Section 2.4.11, "Base Low Page Register 0 (BLOP0)," on page 13) with the exception they are associated with the other DMA channels as indicated by their numeric suffix (i.e. BLOP5 is the Base Low Page Register for DMA channel 5). They have unique addresses as shown in Table 2 on page 5

2.4.13 Current High Page Register 0 (CHIP0)

Table 13. Current High Page Register 0 (CHIP0) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[7]	0x06	Read/Write	undefined	N/A

Each DMA channel has a Current Low Page Register, Base Low Page Register, Current High Page Register and Base High Page Register. The Current High Page Register 0, CHIP0, provides the most significant byte, bits 31-24, of the 32 bit current address for both DMA and Scatter/Gather (S/G) transfers on DMA channel 0. If the Current Low Page Register 0, CLOP0, overflows or underflows during a S/G transfer, the CHIP0 register must be incremented or decremented accordingly. CHIP0 need not increment/decrement during a DMA operation, although some hardware designs may allow it. The Current High Page Register, CHIP0, and the Base High Page Register, BHIP0 (2.4.15 on page 14), are at the same address and are written concurrently.

CHIP0 is set to 0x00 after the Low Page Register (2.4.9 on page 12) is programmed. CHIP0 must be programmed after the Low Page Register.

2.4.14 Current High Page Register 1-7 (CHIP1-CHIP7)

Current High Page Registers 1-7, CHIP1-CHIP7, are identical to Current High Page Register 0 (2.4.13 on page 13) with the exception they are associated with the other DMA channels as indicated by their numeric suffix (i.e. CHIP5 is the Current High Page Register for DMA channel 5). They have unique addresses as shown in Table 2 on page 5

2.4.15 Base High Page Register 0 (BHIP0)

Table 14. Base High Page Register 0 (BHIP0) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[7]	0x06	Write Only	Undefined	N/A

Each DMA channel has a Base High Page Register which holds the initial value programmed into its Current High Page Register. Base High Page Register 0, BHIP0, is the Base High Page Register for channel 0. If autoinitialize is enabled in the DMA Channel Mode register (2.5.3), BHIP0 is copied into CHIP0 after a Terminal Count (TC). During a scatter/gather operation, BHIP0 is used to hold a reserve buffer.

2.4.16 Base High Page Register 1-7 (BHIP1-BHIP7)

Base High Page Registers 1-7, BHIP1-BHIP7, are identical to Base High Page Register 0 (2.4.15 on page 14) with the exception they are associated with the other DMA channels as indicated by their numeric suffix (i.e. BHIP5 is the Base High Page Register for DMA channel 5). They have unique addresses as shown in Table 2 on page 5.

2.5 DMA Controller Registers

2.5.1 DMA 1 Command Register (DCOM1)

Table 15. DMA 1 Command Register (DCOM1) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[1]	0x08	Write Only	0x00	0x00 See 2.5.17 and 2.5.18

This write-only register controls the configuration of DMA Controller 1 which controls DMA channels 0-3. DMA Controller 1 is cascaded through DMA channel 4 of DMA Controller 2. It is cleared by a hardware reset or a write to the Master Clear register described in Section 2.5.17, “DMA 1 Master Clear Register (DMC1),” on page 24.

Table 16. DMA Command Register

Bit	Function
7	Set to 0. In some hardware implementations, bit 7 is the DACK# assert level. This bit determined the polarity of the DACK# signal presented to the ISA bus.
6	Set to 0. In some hardware implementations, bit 6 is the DREQ assert level. This bit determined how signals from the ISA DREQ line are decoded and recognized by the ISA DMA controller.
5	Reserved, set to 0.
4	**DMA Group Arbitration Priority**: Channel groups are assigned either fixed or rotating arbitration priority. When PCIRST# is asserted, this bit assumes a value of 0 and the channel group controlled by DMA controller 1 (channels 0-3) is initialized to fixed priority. When this bit is set to 1, this channel group is assigned rotating priority.
3	Reserved, set to 0.
2	**DMA Channel Group Enable**: When a 1 is written to this bit, the channel group including DMA channels 0-3 is disabled.
1-0	Reserved, set to 0

Requirements:

2–8. For ISA DMA, the DACK# signal must be active low.

2–9. For ISA DMA, the DREQ signal must be active high.

2.5.2 DMA 2 Command Register (DCOM2)

Table 17. DMA 2 Command Register (DCOM2) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[3]	0x10	Write Only	0x00	0x00 See 2.5.17 and 2.5.18

DMA Command Register 2, DCOM2, is identical to the DMA Command Register 1, DCOM1, with the following differences:

1. DCOM2 controls channels 4-7whereas DCOM1 controls channels 0-3.
2. Setting bit 2 in DCOM2, DMA Channel Group Enable, will disable DMA controller 1 which is controlled by DCOM1. Setting bit 2 in DCOM2 will disable DMA channels 0-3 and 4-7.

2.5.3 DMA 1 Channel Mode Register (DCM1)

Table 18. DMA 1 Channel Mode Register (DCM1) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Indirect	reg[1]	0x0B	Write Only	Undefined	N/A

Each DMA channel has a DMA Channel Mode Register. The channel mode registers for channels 0-3 are accessed through DCM1. Bits 1-0 of DCM1 select one of four channels. The value of the DMA Channel Select, bits 1-0, determines which channel mode register bits 7-2 are written to. Writing to DCM1 sets the DMA transfer type, transfer mode, address increment/decrement and autoinitialization for the selected channel.

Table 19. DMA Channel Mode Register

Bit	Function
7-6	**DMA Transfer Mode**: 00 = Demand Mode 01=Single Mode 10=Block Mode 11=Cascade Mode
5	**Address Increment/Decrement Select**. 0=increment, 1=decrement.
4	**Autoinitialize Enable**: When this bit is 1, the DMA controller loads the current low page, current high page, current address and current count information from their respective base registers following a terminal count, TC. When this bit is 0, these registers will not be restored after a TC.
3-2	**DMA Transfer Type** 00=Verify Transfer 01=Write Transfer 10=Read Transfer 11=Illegal

Table 19. DMA Channel Mode Register *(Continued)*

Bit	Function
1-0	**DMA Channel Select** 00=Channel 0 (4) 01=Channel 1 (5) 10=Channel 2 (6) 11=Channel 3 (7)

2.5.4 DMA 2 Channel Mode Register (DCM2)

Table 20. DMA 2 Channel Mode Register (DCM2) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Indirect	reg[3]	0x16	Write Only	Undefined	N/A

This register is identical to the DCM1 with the following two differences:

1. DCM2 controls channels 4-7 whereas DCM1 controls channels 0-3.
2. The DMA Channel Mode Register for channel 4 (indirectly addressed through DCM2) must be set to cascade mode since this channel is used as the cascade for channels 0-3.

2.5.5 DMA 1 Extended Mode Register (DCEM1)

Table 21. DMA 1 Extended Mode Register (DCEM1) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Indirect	reg[5]	0x00	Write Only	0b000000XX	N/A

Each channel has a DMA Extended Mode Register. This register is used to program DMA timing modes. Bits [1:0] select the appropriate Channel Extended Mode Register. DCEM1 is used for channels 0-3. DMA 2 Channel Extended Mode Register (DCEM2) described in Section 2.5.6, “DMA 2 Extended Mode Register (DCEM2),” on page 19 is used for channels 5-7.

Table 22. DMA Extended Mode Register

Bit	Function
7	Must be 0.
6	Must be 0. Was TC (EOP) Input/Output Selection in some hardware designs**:** The architecture only requires TC to be an output of the ISA DMA controller.
5-4	**DMA Cycle Timing Mode**. See Table 23 on page 18

Table 22. DMA Extended Mode Register *(Continued)*

Bit	Function
3-2	**Addressing Mode** Must be set to 0b00 for channels 0-3. (8-bit count by byte addressing mode) Must be set to 0b01 for channels 5-7 (16-bit count by word addressing mode)
1-0	**DMA Channel Select** 00=Channel 0 01=Channel 1 (5) 10=Channel 2 (6) 11=Channel 3 (7)

2.5.5.1 Terminal Count

Requirements:

2–10. For ISA DMA, software must assume the terminal count (TC) is an output from the DMA controller. This means some ISA devices may not work if they depend on TC being an input to the DMA controller.

2–11. For ISA DMA, a hardware design must not produce an error if 0b0 is written to bit 6 of DCEM1 or DCEM2.

2.5.5.2 DMA Timing Modes

Four DMA transfer timings are selectable: ISA compatible, type “A”, type “B”, and type “F”. The timings given assume an ISA SYSCLK of 8.33 Mhz

.

Table 23. DMA Timing Modes

Bits 5-4	DMA Timing Mode
0b00	**ISA-Compatible Timing:** Compatible timing is provided for DMA slave devices that cannot support the higher speed modes (A, B or F). It uses 9 ISA SYSCLKs during a single cycle transfer (1080ns/single cycle). During the repeated portions of BLOCK and DEMAND mode transfers it uses 8 SYSCLKs (960ns/cycle).
0b01	**Type “A” Timing:** The I/O setup portion of the cycle is the same as with compatible timing (9 SYSCLKS - 1080ns/single cycle). During the repeated portions of BLOCK and DEMAND mode transfers type “A” timing uses 6 SYSCLKs (720ns/cycle).
0b10	**Type “B” Timing:** The I/O setup portion of the cycle is the same as with compatible timing (9 SYSCLKS - 1080ns/single cycle). During the repeated portions of BLOCK and DEMAND mode transfers type “B” timing uses 5 SYSCLKs (600ns/cycle).
0b11	**Type “F” Timing:** The I/O setup portion of the cycle is the same as with compatible timing (9 SYSCLKS - 1080ns/single cycle). During the repeated portions of BLOCK and DEMAND mode transfers type “F” timing uses 3 SYSCLKs (360ns/cycle). This is the fastest mode providing 8.33 Mbytes/sec of data transfer.

2.5.5.3 DMA Addressing Modes

DMA Controller 1 is only required to support 8-bit count by byte mode. DMA Controller 2 is only required to support 16-bit count by word (2-byte) mode. The ISA DMA Controller is not required to support 16-bit count by bytes addressing mode.

Requirements:

2–12. For operations involving ISA DMA slave devices, software must assume the hardware only allows addressing modes as follows:

a. Channels 0-3 are 8-bit count by bytes addressing mode. The DMA address, count, and page registers must be programmed accordingly.

b. Channels 5-7 are 16-bit count by word (2 bytes) addressing mode. The DMA address, count, and page registers must be programmed accordingly.

c. 16-bit count by bytes addressing mode is not supported.

2–13. For ISA DMA, a hardware design must not produce an error if 0b00 is written to bits [3:2] of DCEM1, or if 0b01 is written to bits [3:2] of DCEM2.

2.5.6 DMA 2 Extended Mode Register (DCEM2)

Table 24. DMA 2 Extended Mode Register (DCEM2) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Indirect	reg[8]	0x00	Write Only	0b000001XX	N/A

This register is identical to the DCEM1 with the following differences:

1. DCEM2 controls channels 5-7 whereas DCEM1 controls channels 0-3. Bits [1:0] must not be set to 0b00.
2. Bits [3:2] must be written with 0b01 to indicate 16-bit count by word transfers.

2.5.7 DMA 1 Request Register (DR1)

Table 25. DMA 1 Request Register (DR1) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Indirect	reg[1]	0x09	Write Only	0b000000XX	0b000000XX See 2.5.17 and 2.5.18

The host processor can initiate a DMA request on a DMA channel 0-3 by identifying the desired DMA channel in bits 1-0, DMA Channel Select, of this register while setting bit 2, DMA Channel Service Request, to a 1. These requests are treated as if the ISA DREQ signal was asserted for the DMA channel. These host processor initiated requests are non-maskable and subject to prioritization by the priority encoder network.

Table 26. DMA Request Register

Bit	Function
7-3	Reserved (Must be 0)
2	**DMA Channel Service Request**: Writing a zero to this bit resets the system initiated DMA channel request. Writing a one to this bit initiates a DMA channel request on the channel indicated by bits 1-0, DMA Channel Select.
1-0	**DMA Channel Select** 00=Channel 0 01=Channel 1 (5) 10=Channel 2 (6) 11=Channel 3 (7)

2.5.8 DMA 2 Request Register (DR2)

Table 27. DMA 2 Request Register (DR2) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[3]	0x12	Write Only	0b000000XX	0b000000XX See 2.5.17 and 2.5.18

This register is identical to DR1 with the following difference:

1. DR2 initiates DMA requests for channels 5-7 as indicated in Table 23. Bits [1:0] must not be set to 0b00.

2.5.9 DMA 1 Write Single Bit Mask Register (WSM1)

Table 28. DMA 1 Write Single Bit Mask Register (WSM1) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Indirect	reg[1]	0x0A	Write Only	0b000001XX	N/A

Incoming DMA channel service requests (DREQs) for channels 0-3 can be individually enabled and disabled using this register. Upon hardware reset and OF transfer to the OS, all channels are masked.

Table 29. DMA 1 Write Single Bit Mask Register

Bit	Function
7-3	Reserved (Must be 0)
2	**Channel Mask Select**: When this bit is a 1, the DMA channel selected by bits 1-0, DMA Channel Select, will have its DREQ line masked off. The DMA channel will be disabled. When this bit is a 0, the DMA channel selected by the DMA Channel Select field will be enabled.

Table 29. DMA 1 Write Single Bit Mask Register *(Continued)*

Bit	Function
1-0	**DMA Channel Select** 00=Channel 0 (4) 01=Channel 1 (5) 10=Channel 2 (6) 11=Channel 3 (7)

2.5.10 DMA 2 Write Single Bit Mask Register (WSM2)

Table 30. DMA 2 Write Single Bit Mask Register (WSM2) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Indirect	reg[3]	0x14	Write Only	0b000001XX	N/A

This register is identical to WSM1 with the following differences.

1. For DMA Controller 2, WSM2 controls enabling and disabling DMA channels 4-7.
2. For DMA Controller 2, disabling DMA channel 4 will disable channels 0-3 since they are cascaded through channel 4.

Note: Upon hardware reset and OF transfer to the OS, all channels are masked

2.5.11 DMA 1 Write All Mask Bits Register (WAM1)

Table 31. DMA 1 Write All Mask Register (WAM1) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[1]	0x0F	Write Only	0x0F	0x0F See 2.5.17 and 2.5.18

The difference between this register and the DMA 1 Write Single Bit Mask Register, WSM1, is that four DMA channels can be enabled or disabled selectively in one write with the WAM1 register. With WSM1, only one DMA channel can be enabled or disabled at a time.

Table 32. DMA 1 Write all Mask Bits Register

Bit	Function
7-4	Reserved (Must be 0)
3-0	**Channel Mask Select:** For WSM1, bit 0 enables/disables channel 0. (1 disables a channel. 0 enables a channel.) Bit 1 enables/disables channel 1. Bit 2 enables/disables channel 2. Bit 3 enables/disables channel 3.

Requirements:

2–14. Software must assume the DMA Write All Mask Bits Registers (WAM1, WAM2) are write-only.

Note: It is recommended that hardware designs allow this register to be read/write, to facilitate software debug. If it is Read/Write, hardware returns the current value of this register, not the last value written by software (they could be different).

2.5.12 DMA 2 Write All Mask Bits Register (WAM2)

Table 33. DMA 2 Write All Mask Bits Register (WAM2) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[3]	0x1E	Write Only	0x0F	0x0F See 2.5.17 and 2.5.18

This register is identical to WAM1 with the following differences:

1. For DMA Controller 2, bit 0 of the WSM2 enables/disables channel 4. (1 disables a channel. 0 enables a channel.) Bit 1 enables/disables channel 5. Bit 2 enables/disables channel 6. Bit 3 enables/disables channel 7.
2. For DMA Controller 2, disabling DMA channel 4 will disable channels 0-3 since they are cascaded through channel 4.

2.5.13 DMA 1 Status Register (DS1)

Table 34. DMA 1 Status Register (DS1) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[1]	0x08	Read Only	0x00	0x00 See 2.5.17 and 2.5.18

Each DMA controller has a read-only DMA Status Register that indicates which DMA channels have reached terminal count and which DMA channels have a pending DMA request. Bits 3-0 are set to indicate that their corresponding channels have reached terminal count, TC. These four bits are reset when the DMA Status Register is read.

Table 35. DMA 1 Status Register

Bit	Function
7-4	**Channel Request Status:** These bits are set when there is a corresponding DMA request active on the ISA bus. When a valid DMA request is pending for a channel (on the ISA DREQ signal line for the channel), the appropriate bit is set here. For DMA Controller 1, DREQ0 set bits 4, DREQ1 sets bit 5, DREQ2 sets bit 6 and DREQ3 sets bit 7.

Table 35. DMA 1 Status Register *(Continued)*

Bit	Function
3-0	**Channel Terminal Count Status**: When a channel reaches its terminal count, TC, its corresponding bit in this field is set. For DMA Controller 1, channel 0's TC status is on bit 0. Channel 1's TC status is on bit 1. Channel 2's TC status is on bit 2. Channel 3's TC status is on bit 3.

2.5.14 DMA 2 Status Register (DS2)

Table 36. DMA 2 Status Register (DS2) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[3]	0x10	Read Only	0x00	0x00 See 2.5.17 and 2.5.18

This register is identical to DS1 with the following differences:

1. For DMA Controller 2, DREQ5 sets bit 5, DREQ6 sets bit 6 and DREQ7 sets bit 7. DMA channel 4 is the cascade and therefore bit 4 is always 0 for DS2.
2. For DMA Controller 2, Channel 5's TC status is on bit 1. Channel 6's TC status is on bit 2. Channel 7's TC status is on bit 3. Since Channel 4 is the cascade, bit 0 is always 0.

2.5.15 DMA 1 Clear Byte Pointer Register (CBP1)

Table 37. DMA 1 Clear Byte Pointer Register (CBP1) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[1]	0x0C	Write Only	Undefined	N/A

A clear byte pointer command is executed prior to writing new address or count information to the DMA controller or reading current address or count information from the DMA controller. After doing a clear byte pointer command, a read or write to the address or count registers will access the least significant byte. The second access to the same address will give the most significant byte of the address or count. CBP1 is for DMA channels 0-3

Bit 7-0 (Clear Byte Pointer): The content of this register is meaningless. The act of writing to its address accomplishes the clear byte pointer command.

2.5.16 DMA 2 Clear Byte Pointer Register (CBP2)

Table 38. DMA 2 Clear Byte Pointer Register (CBP2) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[3]	0x18	Write Only	Undefined	N/A

This register accomplishes the same purpose as CBP1 with the following exceptions:

1. CBP2 performs the clear byte pointer command for DMA controller 2 which controls channels 5-7.

2.5.17 DMA 1 Master Clear Register (DMC1)

Table 39. DMA 1 Master Clear Register (DMC1) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[1]	0x0D	Write Only	Undefined	N/A

The DMA Master Clear Register 1, DMC1, allows software to perform the equivalent of a hardware reset of DMA Controller 1 (Channels 0-3) under software control. Writing to DMC1resets the Command, Status, Request, and Internal First/Last flip-flop, and sets the Mask Register.

Bit 7-0 (Master Clear): The contents of this register have no meaning. Writing to this register accomplishes a soft reset which is logically equivalent to a hardware reset for DMA controller 1.

2.5.18 DMA 2 Master Clear Register (DMC2)

Table 40. DMA 2 Master Clear Register (DMC2) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[3]	0x1A	Write Only	Undefined	N/A

This register, is identical to DMC1 with the following differences:

1. For DMA Controller 2 (Channels 4-7), DMC2 performs the equivalent of a hardware reset.

2.5.19 DMA 1 Clear Mask Register (DCLM1)

Table 41. DMA 1 Clear Mask Register1 (DCLM1) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[1]	0x0E	Write Only	Undefined	N/A

Writing to this register clears any masks which may be in place for DMA channels 0-3. The value of the data for the write is irrelevant.

2.5.20 DMA 2 Clear Mask Register (DCLM2)

Table 42. DMA 2 Clear Mask Register (DCLM2) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[3]	0x1C	Write Only	Undefined	N/A

Writing to this register clears any masks which may be in place for DMA channels 4-7. The value of the data for the write is irrelevant.

2.6 Scatter/Gather Registers

Requirements:

2–15. During Scatter/Gather operations, the High Page Registers (described in Section 2.4.13, “Current High Page Register 0 (CHIP0),” on page 13 through Section 2.4.14, “Current High Page Register 1-7 (CHIP1-CHIP7),” on page 14) and Low Page Registers (described in Section 2.4.9, “Current Low Page Register 0 (CLOP0),” on page 12 through Section 2.4.10, “Current Low Page Register 1-7 (CLOP1-CLOP7),” on page 13) must increment appropriately as part of the full 32 bit transfer address.

2.6.1 The Scatter/Gather Descriptor

Figure 2 on page 26 gives the format of the Scatter/Gather Descriptor (abbreviated as SGD). A contiguous list of SGD’s in real memory makes up a SGD Table. A SGD must be aligned on a 4-byte boundary.

DWORD0 of a SGD contains the address of a buffer in memory that is to be transferred to or from an ISA I/O device. If the transfer mode of the operation is 16-bit count by word, (i.e. one of channels 5-7 is used), then the address of that buffer must be even (the lsb of the address is 0).

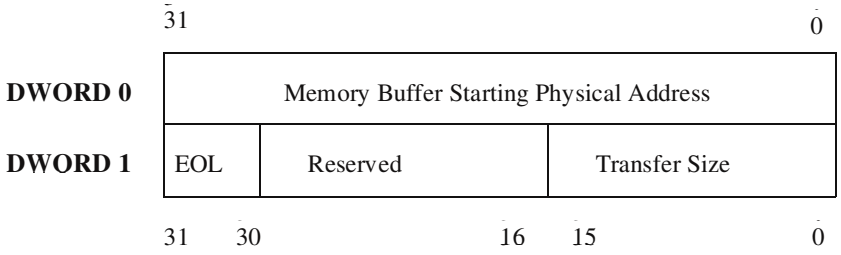
Requirements:

2–16. Scatter/Gather Descriptor: The Memory Buffer Starting Physical Address field in the SGD must be programmed as follows:

a. For 8-bit count by byte operations, this field is programmed with the byte address of the buffer to be transferred. The address may be even or odd.

b. For 16-bit count by word operations, this field is programmed with the *even* byte address of the buffer to be transferred. Thus, bit 0 in this field will be 0.

The Transfer Size field gives the number of bytes or 16 bit words to be transferred. The last SGD in a scatter/gather program must have the EOL field set to 1 to signal that it is the last entry.



Entries in system memory are in LE format.

Figure 2. Scatter Gather Descriptor Table Entry

2.6.2 Scatter/Gather Interrupt Status Register (SGIS)

Table 43. Scatter/Gather Interrupt Status Register (SGIS) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[4]	0x00	Read Only	0x00	N/A

The Scatter/Gather Interrupt Status Register indicates the DMA channel which is the source of a DMA Scatter/Gather interrupt on IRQ13 of the Legacy Interrupt Controller (see Chapter 4, “Legacy Interrupt Controller,” on page 61). The DMA controller drives IRQ13 active after it reaches a terminal count during a Scatter/Gather DMA operation, if bits [7:6] of the Scatter/Gather Command Register are 0b01 (Section 2.6.3, “Scatter/Gather Command Register 0 (SGC0),” on page 27).

Requirements:

2–17. IRQ 13 must be reserved for the ISA DMA device.

Table 44. Scatter/Gather Interrupt Status Register (SGIS)

Bit	Function
7	1=interrupt pending on channel 7. 0=no interrupt pending.
6	1=interrupt pending on channel 6. 0=no interrupt pending.
5	1=interrupt pending on channel 5. 0=no interrupt pending.
4	Reserved (Must be 0)
3	1=interrupt pending on channel 3. 0=no interrupt pending.
2	1=interrupt pending on channel 2. 0=no interrupt pending.
1	1=interrupt pending on channel 1. 0=no interrupt pending.
0	1=interrupt pending on channel 0. 0=no interrupt pending.

2.6.3 Scatter/Gather Command Register 0 (SGC0)

Table 45. Scatter/Gather Command Register 0 (SGC0) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[6]	0x00	Write Only	0x00	N/A

The Scatter/Gather Command Register 0 (SGC0) provides commands to start and halt scatter/gather operations on DMA channel 0 and TC to set the method of how the end of the scatter/gather operation will be signalled.

Table 46. Scatter/Gather Command Register 0 (SGC0)

Bit	Function
7	**IRQ13/TC Select:** This bit selects whether Terminal Count (TC) or IRQ13 is asserted when the last buffer in a scatter/gather list has been completed or the last buffer in the DMA has been completed after the DMA has been suspended (a terminal count has occurred). A 1 selects TC as the signaling mechanism. A 0 selects IRQ13 as the signaling mechanism. This bit is only valid if bit 6, IRQ13/TC Programming Enable, is a 1.
6	**IRQ13/TC Programming Enable:** When this bit is a 0, bit 7 does not affect the current state of whether TC or IRQ13 is being used to signal the end of a scatter/gather operation as noted under bit 7. When bit 6 is a 1, bit 7 is enabled to change the state of how the DMA controller signals a terminal count.
5-2	Reserved (Must be set to 0)
1-0	**Scatter/Gather Commands.** See Table 47 on page 27.

Table 47. Scatter/Gather Commands

Bits 1-0	Scatter/Gather Commands
00	**No S/G Operation:** No Scatter/Gather operation is performed. This is typically used when it is desired to change bits 6 and 7.

Table 47. Scatter/Gather Commands *(Continued)*

Bits 1-0	Scatter/Gather Commands
01	**Start S/G Command:** This command initiates the scatter/gather DMA operation. The DMA controller will begin fetching entries from the Scatter/Gather Descriptor table immediately upon the setting of this bit. When this command is used, all base address, base word, current address and current word registers should be empty (unused).
10	**Stop S/G Command:** This command halts a scatter/gather transfer immediately. Bits 0, 2, 3, and 5 in the Scatter/Gather Status Register (2.6.5)are cleared to 0 and the DMA channel mask bit in the WAM0 or WAM1 register is set to 1. (WAM0 for channels 0-3, WAM1 for channels 5-7)
11	Reserved

2.6.4 Scatter/Gather Command Registers 1-7 (SGC2-SGC7)

Scatter/Gather Command Registers 1-7, SGC1-SGC7, are identical to Scatter/Gather Command Register 0, SGC0, with the exception they control different DMA channels as indicated by the suffixes on the register names and abbreviations. They have unique addresses as shown in Table 2 on page 5

2.6.5 Scatter/Gather Status Register 0 (SGS0)

Table 48. Scatter/Gather Status Register 0 (SGS0) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
1 byte	Direct	reg[6]	0x08	Read Only	0x00	0bX0000000 See 2.6.3

This register provides status information on the Scatter/Gather unit for a given DMA channel, in this case, channel 0.

Table 49. Scatter/Gather Status Register 0 (SGS0)

Bit	Function
7	**Next Link Null Indicator:** If the next SGD fetched has an EOL value of 1, it is the last SGD in the scatter/gather list in memory for this scatter/gather operation. When EOL is a 1 in the next SGD, bit 7 is set to a 1.
6	Reserved
5	Reserved.
4	Reserved
3	**Scatter/Gather Base Register Status**: When this bit is a 0, the DMA Base Address Register is empty. When it is a 1, a buffer is pre-loaded (the next link in the SGD table) in the DMA Base Address Register for this channel.
2	**Scatter/Gather Current Register Status**: When this bit is a 0, the DMA Current Address Register is empty. When it is a 1, a buffer is loaded (the current link in the SGD table) in the DMA Current Address Register for this channel.
1	Reserved

Table 49. Scatter/Gather Status Register 0 (SGS0) ***(Continued)***

Bit	Function
0	**Scatter/Gather Active:** This bit indicates the status of a current scatter/gather DMA operation. When this bit is a 1, a scatter/gather start command has been issued. When this bit is set to 0, no operation is in progress, a terminal count on the last buffer in the SGD list has occurred or a scatter/gather stop command has been issued.

2.6.6 Scatter/Gather Status Register 1-7 (SGS1-SGS7)

Scatter/Gather Status Registers 1-7, SGS1-SGS7, are identical to Scatter/Gather Status Register 0, SGS0, with the exception they present status for different DMA channels as indicated by the suffixes on the register names and abbreviations. They have unique addresses as shown in Table 2 on page 5.

2.6.7 Scatter/Gather Descriptor Table Pointer Register 0 (SGPTR0)

Table 50. Scatter/Gather Descriptor Table Pointer Register 0 (SGPTR0) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register When OF Passes Control to OS	Software Initiated Reset Value
4 byte	Direct	reg[6]	0x10-0x13	Read/Write	Undefined	N/A

This register contains a 32-bit address for scatter/gather channel 0 that points to the first Scatter/Gather Descriptor, SGD, in a list in system memory. This register is programmable using a single 32 bit write. The SGD list and this register must be programmed (in addition to other things) prior to the issue of the scatter/gather start command.

Bits [31:0] of this register correspond to bits [31:0] on the PCI bus.

Requirements:

2–18. The Scatter/Gather Descriptor Table Pointer Registers must be programmed with a single 32-bit write.

2.6.8 Scatter/Gather Descriptor Table Pointer Registers 1-7 (SGPTR1-SGPTR7)

Scatter/Gather Descriptor Table Pointer Registers 1-7, SGPTR1-SGPTR7, are identical to Scatter/Gather Descriptor Pointer Register 0, SGPTR0, with the exception they service different DMA channels as indicated by the suffixes on the register names and abbreviations. They have unique addresses as shown in Table 2 on page 5.

2.7 Support for ISA Bus masters

ISA bus masters may operate using any of the seven available DMA channels, regardless of transfer width. (ISA bus masters provide their own address and count information.)

Requirements:

2–19. The ISA DMA Controller must not preclude an ISA bus master from using any of the seven available DMA channels, regardless of addressing mode.

2–20. The ISA DMA hardware must provide at least 24-bit addressing to system memory for ISA bus masters.

When programming for an ISA bus master operation, only two registers are used in the ISA DMA controller,

1. Channel Mode register (DCM1, DCM2). This puts the desired channel into cascade mode.
2. Write Single Bit Mask register (WSM1, WSM2). This is used to unmask the desired channel.

Note: some hardware designs allow the High Page Register to form the high-order address bits of a 32-bit ISA bus master PCI address.

During an ISA bus master operation, many of the DMA and all of the S/G registers described in previous sections are not used. These include:

1. Current Address Registers
2. Base Address Registers
3. Current Count Registers
4. Base Count Registers
5. Current Low Page Register
6. Base Low Page Register
7. Extended Mode Register
8. Clear Byte Pointer Register

Floppy Disk Controller

3

3.1 General Requirements

Table 51 on page 31 is an excerpt from *PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture*, showing the minimum requirements of the floppy disk controller on CHRP platforms.

Table 51. Summary of Minimum Platform Requirements

Subsystem	Specification	Portable	Personal	Server	Description
Floppy		O	O	O	Not required, but a means to attach for software installation must be provided. This may be through a provided connector or over a network. Media sense: Implementations must allow polling of the drive up to 100x per second to determine the presence of media in the drive. A method for manual ejection of floppies is required.
	3.5" 1.44 MB MFM	R	R	R	
	Media sense	R	R	R	
	Auto eject	R	R	M	
	Manual eject	R	R	R	

Requirements:

3–1. A Floppy Disk Controller that is compliant with the interfaces as defined in this section must be represented in the Open Firmware device tree for the auto-eject version of the device as identified by the following properties; name=fdc, device_type=fdc, and compatible=chrp,fdc. For the non-auto-eject version of the device, it is represented by the following properties; name=fdc, device_type=fdc, and compatible=pnpPNP,700.

3–2. The firmware must configure the Floppy Disk Controller in the PS/2™ mode, with enhanced auto-eject or without auto-eject.

3–3. This device must be addressed purely with ISA I/O addresses which can be aliased or non-aliased.

3–4. DMA transfers for the floppy disk controller must be 8-bit DMA slave and must support at least the ISA Compatible Timing mode.

3–5. Interrupts generated by the floppy disk controller must be high true edge sensitive.

Software Implementation Note: The PS/2 mode controllers only support two drives.

Software Implementation Note: The operating system is expected to extract the DMA channel number from the node's dma property. The above requirement means that the operating system need not extract the DMA transfer size, DMA count width, or master vs slave capability from the node's dma property. Firmware must set these fields to the values that match the above requirement. Operating systems are recommended to

extract the DMA timing from the node's DMA property, though they are free to default to the ISA Compatibility Timing Mode. Refer to Table 23 on page 18 for information about other timing modes.

Software Implementation Note: The operating system is expected to extract the interrupt number from the node's interrupts property. The above requirement means that the operating system need not extract the interrupt type from the node's interrupts property. Firmware must set this field to the values that match the above requirement.

Hardware Implementation Note: The Floppy interrupts are not tri-stated but left enabled, unlike CHRP requirement 2-1.

3.2 Floppy Disk/Tape Media Supported

Requirements:

3–6. The floppy disk controller must support 3.5 inch media with an unformatted capacity of 2 megabytes and a formatted capacity of 1.44 megabytes.

3–7. The floppy disk controller must support the 3.5 inch media with an unformatted capacity of 4 megabytes and a formatted capacity of 2.88 megabytes for purposes of floppy disk port tape backup units.

It is recommended that the floppy disk controller support 3.5 inch media with an unformatted capacity of 1 megabytes and a formatted capacity of 720 kilobytes to enable the use of legacy media of that density.

3.3 Floppy Disk Controller Open Firmware Properties

Requirements:

3–8. The three sets of registers shown in Table 52 on page 33 must be present in the Open Firmware device tree for the auto-eject version of the device as identified by the following properties; name=fdc, device_type=fdc, and compatible=chrp,fdc.

3–9. The first two sets of registers shown in Table 52 on page 33 must be present in the Open Firmware device tree for the non-auto-eject version of the device as identified by the following properties; name=fdc, device_type=fdc, and compatible=pnpPNP,700.

3–10. This device must be represented as an ISA device and a child of an ISA bridge node in the Open Firmware device tree.

3–11. A floppy disk controller must be reported in the Open Firmware device tree as specified in the *CHRP ISA Floppy Device Binding* [16].

Table 52 on page 33 gives the registers used by the floppy disk controller.

Table 52. Floppy Disk Controller Registers

Offset	Register	Open Firmware Reg Property
0	Status Register A (SRA)	(reg[1], size = 6)
1	Status Register B (SRB)	
2	Digital Output Register (DOR)	
3	Tape Drive Register (TDR)	
4	Main Status Register (MSR)/ Data Rate Select Register (DSR)	
5	Data Register (FIFO)	
0	Digital Input Register (DIR)/ Configuration Control Register (CCR)	(reg[2], size = 1)
0	Autoeject Register (AER)	(reg[3], size = 1)

3.4 Diskette Drive Controller Registers

Requirements:

3–12. For the device described herein, all the registers defined in Section 3.4.1, “Status Register A (SRA),” on page 33 through Section 3.4.10, “Autoeject Register (AEJ),” on page 41 must be implemented as described herein.

Two sets of registers are described here, control and status. The control registers each have a unique offset address. Floppy disk operations are split into command, execution and result phases. During the result phase, the status registers described are read through the Data Register FIFO (abbreviated as FIFO).

3.4.1 Status Register A (SRA)

Table 53. Status Register A (SRA) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value when OF passes to SW	Software Reset Value
1 byte	Direct	reg[1]	0x00	Read Only	See Table 54 on page 33	See Table 54 on page 33

Status Register A, SRA, monitors the state of the floppy disk interrupt source and some of the disk interface signals.

Table 54. Status Register A (SRA)

Bit	Function	Value when OF passes to SW	Value After Software Reset
7	**Interrupt Pending:** This active high bit reflects the state of the interrupt source from the floppy disk controller.	0	0

Table 54. Status Register A (SRA)

Bit	Function	Value when OF passes to SW	Value After Software Reset
6	**Reserved**	x	x
5	**Step:** Active high bit reflecting the state of the STEP disk interface output.	0	0
4	**-Track 0:** Active low bit reflecting the status of the TRK0 disk interface input.	x	x
3	**Head Select:** Active high bit reflecting the status of the HDSEL disk interface output.	0	0
2	**-Index:** Active low bit reflecting the INDEX disk interface input.	x	x
1	**-Write Protect:** Active low bit reflecting the WP disk interface input.	x	x
0	**Direction:** Active high bit reflecting the DIR disk interface output.	0	0

3.4.2 Status Register B (SRB)

Table 55. Status Register B (SRB) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Wrt Characteristics	Value when OF passes to SW	Software Reset Value
1 byte	Direct	reg[1]	0x01	Read Only	See Table 56 on page 34	See Table 56 on page 34

This read-only register shows the status of signals on the diskette drive interface. The write-data and read-data bits change state for each positive transition of the ‘-write data’ or ‘-read data’ signals.

Table 56. Status Register B

Bit	Function	Value when OF passes to SW	Value After Software Reset
7,6	**Reserved**	x	x
5	**Drive Select 0:** Reflects the status of the Drive Select 0 bit in the DOR, Digital Output Register (address2, bit 0). It is cleared after a hardware reset, not a software reset.	x	x
4	**Write Data:** Every inactive edge transition of the WDATA disk interface output causes this bit to change state.	0	0
3	**Read Data:** Every inactive edge transition of the RDATA disk interface output causes this bit to change states.	0	0
2	**Write Gate:** Active high bit reflecting the WGATE interface output.	0	0
1	**Motor Enable 1:** Active high bit reflecting the status of the MTR1 disk interface output.	0	x
0	**Motor Enable 0:** Active high bit reflecting the status of the MTR0 disk interface output.	0	x

3.4.3 Digital Output Register (DOR)

Table 57. Digital Output Register (DOR) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Wrt Characteristics	Value when OF passes to SW	Software Reset Value
1 byte	Direct	reg[1]	0x02	Read/Write	See Table 58 on page 35	See Table 58 on page 35

The Digital Output Register, DOR, controls the drive select and motor enable disk interface outputs, enables the DMA logic, and contains a software reset bit.

Table 58. Drive Control Register

Bit	Function	Value when OF passes to SW	Value After Software Reset
7	**Motor Enable 3:** This bit controls the MTR3 disk interface output. A 1 in this bit causes the MTR3 pin to go active.	0	x
6	**Motor Enable 2:** This bit controls the MTR2 disk interface output. A 1 in this bit causes the MTR2 pin to go active.	0	x
5	**Motor Enable 1:** This bit controls the MTR1 disk interface output. A 1 in this bit causes the MTR1 pin to go active.	0	x
4	**Motor Enable 0):** This bit controls the MTR0 disk interface output. A 1 in this bit causes the MTR0 pin to go active.	0	x
3	**Reserved**	0	x
2	**-Reset Controller):** Writing a 0 to this bit resets the controller. It remains in the reset condition until a 1 is written to this bit. Software resets do not affect the DSR, CCR and other bits of the DOR. This bit must be 0 for at least 100ns before a 1 can be written to it.	0	x
1-0	**Drive Select:** These two bits are a binary encoding of the four drive selects DR0-DR3. This insures that only one drive select output can be active at a time.	0	x

N/A as the value after soft reset means that the bit value is not affected.

3.4.4 Tape Drive Register (TDR)

Table 59. Tape Drive Register (TDR) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Wrt Characteristics	Value when OF passes to SW	Software Reset Value
1 byte	Direct	reg[1]	0x03	Read/Write	See Table 60 on page 36	See Table 60 on page 36

The TDR register is the Tape Drive Register and the floppy disk controller media and drive type register. Only what has been called the “enhanced” mode of operation is supported and documented here.

Table 60. Drive Status Register

Bit	Function	Value when OF passes to SW	Value After Software Reset
7	**Extra Density:** When bit 5 is 0, this media id bit is used with bit 6 as described in Table 61 on page 36 to indicate the type of media currently in the floppy drive	x	x
6	**High Density:** When bit 5 is 0, this media id bit is used with bit 7 as described in Table 61 on page 36 to indicate the type of media currently in the floppy drive.	x	x
5	**Drive ID 1 Information:** The state of this bit is determined by the state of bits 1 and 0 in the Drive ID register. If this bit is 0, there is valid media ID sense data in bits 7 and 6 of this register. This bit holds the value of bit 1 of the Drive ID register, when drive 0 is accessed and media sense is configured. It holds the value of bit 3 of the Drive ID register, when drive 1 is accessed and media sense is configured. Otherwise, it is set to 1 to indicate that media information is not available. Valid data should be used only when accessing drives 0 and/or 1. Table 61 on page 36 shows what the decoded interpretations of bits 7-5 mean.	x	x
4	**Drive ID 0 Information:** This bit reflects the value of bit 0 in the Drive ID Register if floppy disk device 0 is accessed. It reflects the value of bit 2 in the Drive ID Register if floppy disk device 1 is accessed	x	x
3-2	**Logical Drive Exchange:** These bits are reserved, and must be set to zero.	0	0
1-0	**Tape Select 1,0:** These bits assign a logical drive number to a tape drive. Drive 0 must remain as a boot drive and cannot be assigned as a tape drive. Table 62 on page 36 shows how these bits assign logical drive numbers to tape drives	0	0

Table 61. Media ID Bit Functions

Bit 7, 6,5	Media Type
X X 1	Invalid Data
0 0 0	5.25 in
0 1 0	2.88 Megabyte (formatted)
1 0 0	1.44 Megabyte (formatted)
1 1 0	720 Kilobyte (formatted)

Software Implementation Note: The Drive ID register in Table 60 on page 36, is not part of the Floppy Disk Controller register set. It is a register where the chipset involved has stored the Drive IDs for drive 0 and drive 1 on the floppy disk interface. It then makes this information available to the Floppy Disk Controller.

Table 62. Tape Drive Assignment Values

Bit 1,0	Drive Selected
00	None
01	1
10	2
11	3

3.4.5 Main Status Register (MSR)

Table 63. Main Status Register (MSR) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value when OF passes to SW	Software Reset Value
1 byte	Direct	reg[1]	0x04	Read Only	0x00	0x00

This read-only register facilitates the transfer of data between the system microprocessor and the controller.

Table 64. Diskette Drive Controller Status Register

Bit	Function	Value when OF passes to SW	Value on Software Reset
7	**Request for Master:** When this bit is 1, the Data register is ready to transfer data with the system microprocessor	0	0
6	**Data Input/Output:** This bit indicates the direction of data transfer between the diskette drive controller and the system microprocessor. When this bit is 1, the transfer is to the system microprocessor; when the bit is 0, the transfer is to the controller	0	0
5	**Non-DMA Mode:** When this bit is 1, the controller is in the non-DMA mode	0	0
4	**Command in Progress:** When this bit is 1, command is being processed.	0	0
3	**Drive 3 Busy:** When this bit is 1, diskette drive 3 is in the seek mode.	0	0
2	**Drive 2 Busy:** When this bit is 1, diskette drive 2 is in the seek mode	0	0
1	**Drive 1 Busy:** When this bit is 1, diskette drive 1 is in the seek mode	0	0
0	**Drive 0 Busy:** When this bit is 1, diskette drive 0 is in the seek mode	0	0

3.4.6 Data Rate Select Register (DRS)

Table 65. Data Rate Select Register (DRS) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value when OF passes to SW	Software Reset Value
1 byte	Direct	reg[1]	0x04	Write Only	SeeTable 66 on page 38	See Table 66 on page 38

This write-only register is used to select the data rate and precompensation value for each data rate.

Table 66. Precompensation Select Register

Bit	Function	Value when OF passes to SW	Software Reset Value
7	**S/W Reset:** This bit functions the same as the POR Reset bit, except it is self clearing.	0	Not effected
6	**Low Power:** This bit puts the floppy disk controller into low power mode. What low power means can vary from manufacturer to manufacturer. The floppy disk controller comes out of low power mode after a software reset, or access to the Data Register or Main Status Register.	0	Not effected
5	**Reserved:** Must be Set to 0.	0	Not effected
4-2	**Precompensation Select:** These bits select the amount of write precompensation the floppy disk controller uses when writing bits to the floppy disk drive. Table 67 on page 38 shows the pre-compensation values for each bit encoding. Table 69 on page 39 shows the default precompensa-tion values for each data rate.	0	Not effected
1-0	**Data Rate Select:** These bits set the data rate of the floppy disk controller. Table 69 on page 39 shows how data rates for the floppy disk controller are encoded	0	Not effected

Table 67. Precompensation Values

Bits 4 3 2	Precompensation Delay
000	Default
001	41.7 ns
010	83.3 ns
011	125.0 ns
100	166.7 ns
101	208.3 ns
110	250 ns
111	0.0 ns

Table 68. Default Precompensation Values

Transfer Rate	Default Precompensation
500Kbps	125ns
300Kbps	125ns
250Kbps	125ns
1000Kbps	41.7ns

Table 69. Data Rate Select Encodings

Bits 1 0	Data Rate	
	MFM	FM
00	500Kbps	250 Kbps
01	300Kbps	150 Kbps
10	250 Kbps	125 Kbps
11	1 Mbps	Illegal

3.4.7 Data Register (FIFO)

Table 70. Data Register (FIFO) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Wrt Characteristics	Value when OF passes to SW	Software Reset Value
1 byte	Direct	reg[1]	0x05	Read/Write	0x00	0x00

The FIFO (read/write) is used to transfer all commands, data and status between the system and the floppy disk controller. During the command phase, the system writes the command bytes into the FIFO after polling the RQM and DIO bits in the MSR. During the result phase, the system reads the result bytes from the FIFO after polling the RQM and DIO bits in the MSR.

Enabling the FIFO, and setting the FIFO threshold, is done via the Configure command. If the FIFO is enabled, only the execution phase byte transfers use the 16 byte FIFO. The FIFO is always disabled during the command and result phases of a controller operation. If the FIFO is enabled, it is not disabled after a software reset if the LOCK bit is set in the lock command. After a hardware reset, the FIFO is disabled to maintain compatibility with PC-AT systems.

The 16-byte FIFO can be used for DMA, Interrupt, or software polling type transfers during the execution of a read, write, format, or scan command. In addition, the FIFO can be put into a burst or non-burst mode with the mode command. In the burst mode, DRQ or IRQ remains active until all of the bytes have been transferred to or from the FIFO. In the non-burst mode, DRQ or IRQ is deasserted for 350 ns to allow higher priority transfer requests to be serviced. The mode command can also disable the FIFO for either reads or writes separately. The FIFO allows the system a larger latency without causing a disk overrun/underrun error. Typical uses of the FIFO are at the 1 Mbit/s data rate, or with multi-tasking operating systems. The default state of the FIFO is disabled, with a threshold of zero. The default state is entered after a hardware reset.

During the execution phase of a command involving data transfer to/from the FIFO, the software must respond to a data transfer service request based on the following formula:

$$(THRESH + 1) \times 8 \times TDRP - (16 \times TICP)$$

This formula is good for all data rates with the FIFO enabled or disabled. THRESH is a four bit value programmed in the configure command, which sets the FIFO threshold. If the FIFO is disabled, THRESH is zero in the above formula. The last term of the formula, (16xTICP) is an inherent delay due to the microcode overhead required by the FDC. This delay is also data rate dependent.

The programmable FIFO threshold (THRESH) is useful in adjusting the floppy controller to the speed of the system. In other words, a slow system with a sluggish DMA transfer service request (DRQ for DMA mode or IRQ for interrupt mode). Conversely, a fast system with quick response to a data transfer service request uses a low value of THRESH.

Table 71 on page 40 is a table of TDRP and TICP values.

TDRP - Data Rate Period

TICP - Internal Clock Period

TCP - Clock Period

Table 71. Floppy FIFO Table

MFM Data Rate	TDRP	TICP	Example TICP Values
1 Mbps	1000	3 X TCP	125 ns
500 Kbps	2000	3 X TCP	125 ns
300 Kbps	3333	5 X TCP	208 ns
250 Kbps	4000	6 X TCP	250 ns

3.4.8 Digital Input Register (DIR)

Table 72. Digital Input Register (DIR) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value when OF passes to SW	Software Reset Value
1 byte	Direct	reg[2]	0x00	Read Only	See Table 73 on page 40	See Table 73 on page 40

Table 73. Diskette Drive Controller Status Register

Bit	Function	Value when OF passes to SW	Value on Software Reset
7	**Disk In Place:** When this bit is a 1 it reflects that the disk is in place.	x	x
6-3	**Reserved.** Must be set to 0b0000.	x	x
2,1	**Data Rate Select:** These bits indicate the status of the DRATE1-0 bits programmed throught the DSR or CCR	x	x
0	**(-High Density):** This bit is a 0 when the 1 Mb/s or 500 Kbps data rate is chosen, and a 1 when the 300 Kbps or 250 Kbps data rate is chosen.	x	x

3.4.9 Configuration Control Register (CCR)

Table 74. Configuration Control Register (CCR) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Wrt Characteristics	Value when OF passes to SW	Software Reset Value
1 byte	Direct	reg[2]	0x00	Write Only	See Table 75 on page 41	See Table 75 on page 41

This write-only register sets the transfer rate.

Table 75. Data Rate Control Register

Bit	Function	Value when OF passes to SW	Value on Software Reset
7-2	**Reserved:** Must be 0	x	x
1	**Data Rate Select:** Bits 1-0 select the data rate, as shown in the Table 76 on page 41	1	1
0	**Data Rate Select:** Bits 1-0 select the data rate, as shown in the Table 76 on page 41	0	0

Table 76. Data Rate Selection

Bits 1 0	Data Rate
00	500,000 bits per second
01	300,000 bits per second
10	250,000 bits per second
11	1,000,000 bits per second*

3.4.10 Autoeject Register (AEJ)

Table 77. Autoeject Register (AEJ) Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value when OF passes to SW	Software Reset Value
1 byte	Direct	reg[3]	0x00	Read/Write	0x00	0x00

This table is provided for systems that optionally support floppy disk auto-eject.

The motor must be stopped before doing an eject. To cause an auto-eject, software must write to the least significant bit of this register with a 1, followed by a pause provided by software of at least 10 microseconds, followed by a write

of a 0, which will result in the auto-eject. All other bits in this register are reserved, therefore software must use a read-modify-write.

3.5 Floppy Drive Controller Programming Considerations

Each command is initiated by a multibyte transfer from the system microprocessor; the result can be a multibyte transfer back to the system microprocessor. Most transfers consist of three phases:

- *Command Phase:* The system microprocessor writes a series of command bytes to the controller directing it to perform a specific operation.
- *Execution Phase:* The controller performs the specified operation.
- *Result Phase:* After the operation is complete, status information is available to the system microprocessor through a sequence of read commands.

The Seek, Relative Seek, and Recalibrate commands have no result phase. After issuing these commands, the Sense Interrupt Status command must be issued for proper termination and verification of the head position (Present Cylinder Number parameter or PCN).

3.5.1 Controller Commands

Requirements:

3–13. For the device described herein, the commands described in Section 3.5.1.1, “Configure Command,” on page 43 through Section 3.5.1.22, “Write Deleted Data Command,” on page 55 must be implemented as specified.

The following are supported commands for diskette drive controller:

- Configure
- Dumpreg
- Format Track
- Lock
- Perpendicular Mode
- Read Data
- Read Deleted Data
- Read ID
- Read Track
- Recalibrate
- Relative Seek
- Scan Equal
- Scan High or Equal

- Scan Low or Equal
- Seek
- Sense Drive Status
- Sense Interrupt Status
- Specify
- Verify
- Version
- Write Data
- Write Deleted Data.
- Invalid Command Status

3.5.1.1 Configure Command

3.5.1.1.1 Command Phase

Table 78. Configure Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	1	0	0	1	1
Byte 1	0	0	0	0	0	0	0	0
Byte 2	0	EIS	EFF	PD	Thresh-old (THR)			
Byte 3	Precompensation Track Number (PTN)							

3.5.1.1.2 Execution Phase

Internal registers are read.

3.5.1.1.3 Result Phase

This command has no result phase.

3.5.1.2 Dumpreg Command

3.5.1.2.1 Command Phase

Table 79. Dumpreg Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	1	0

3.5.1.2.2 Execution Phase

Internal registers are written.

3.5.1.2.3 Result Phase

Table 80. Dumpreg Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Present Track Number - Drive 0							
Byte 1	Present Track Number - Drive 1							
Byte 2	Present Track Number - Drive 2							
Byte 3	Present Track Number - Drive 3							
Byte 4	Stepping Rate Time Head Unload Time							
Byte 5	Head Load Time							DMA
Byte 6	Number of Sectors per Track/End of Track							
Byte 7	X	0	Reserved			X	GAP	WGATE
Byte 8	O	EIS	EFF	PD	Threshold			
Byte 9	Precompensation Track Number							

3.5.1.3 Format Track Command

3.5.1.3.1 Command Phase

Table 81. Format Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	MFM	0	0	1	1	0	1
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Number of Data Bytes in Sector							
Byte 3	Sectors per Track							
Byte 4	Gap Length							
Byte 5	Fill Byte							

3.5.1.3.2 Execution Phase

The system transfers four ID bytes (track, head, sector, bytes/sector) per sector to the floppy controller via DMA or Non-DMA modes. The entire track is formatted. The data block in the data field of each sector is filled with the data pattern byte.

3.5.1.3.3 Result Phase

Table 82. Format Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Reserved
Byte 4	Reserved
Byte 5	Reserved

Table 82. Format Result Phase *(Continued)*

Byte 6	Reserved

3.5.1.4 Lock Command

3.5.1.4.1 Command Phase

Table 83. Lock Command Phase

	7	6	5	4	3	2	1	0
Byte 0	Lock	0	0	1	0	1	0	0

3.5.1.4.2 Execution Phase

An internal Register is written.

3.5.1.4.3 Result Phase

Table 84. Lock Result Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	Lock	0	0	0	0

3.5.1.5 Perpendicular Mode Command

3.5.1.5.1 Command Phase

Table 85. Perpendicular Mode Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	1	0	0	1	0
Byte 1	OW	0	D3	D2	D1	D0	GAP	WGATE

3.5.1.5.2 Execution Phase

Internal registers are written.

3.5.1.5.3 Result Phase

There is no result phase for the Perpendicular Mode command.

3.5.1.6 Read Data Command

3.5.1.6.1 Command Phase

Table 86. Read Data Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT0	MFM	SK	0	0	1	1	0
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Track Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End-of-Track							
Byte 7	Gap Length							
Byte 8	Data Length							

3.5.1.6.2 Execution Phase

Data read from disk drive is transferred to system via DMA or non-DMA modes.

3.5.1.6.3 Result Phase

Table 87. Read Data Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Track Number
Byte 4	Head Address
Byte 5	Sector Number
Byte 6	Number of Data Bytes in Sector

3.5.1.7 Read Deleted Data Command

3.5.1.7.1 Command Phase

Table 88. Read Deleted Data Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MFM	SK	0	1	1	0	0
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Track Number							
Byte 3	Head Address							
Byte 4	Sector Number							

Table 88. Read Deleted Data Command Phase *(Continued)*

	7	6	5	4	3	2	1	0
Byte 5	Number of Data Bytes in Sector							
Byte 6	End-of-Track							
Byte 7	Gap Length							
Byte 8	Data Length							

3.5.1.7.2 Execution Phase

Data read from disk drive is transferred to system via DMA or non-DMA modes.

3.5.1.7.3 Result Phase

Table 89. Read Deleted Data Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Track Number
Byte 4	Head Address
Byte 5	Sector Number
Byte 6	Number of Data Bytes in Sector

3.5.1.8 Read ID Command

3.5.1.8.1 Command Phase

Table 90. Read ID Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	MFM	0	0	1	0	1	0
Byte 1	0	0	0	0	0	HD	US	US

3.5.1.8.2 Execution Phase

The controller reads the first ID field header bytes it can find and reports these bytes to the system in the result bytes.

3.5.1.8.3 Result Phase

Table 91. Read ID Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Track Number
Byte 4	Head Address

Table 91. Read ID Result Phase *(Continued)*

Byte 5	Sector Number
Byte 6	Number of Data Bytes in Sector

3.5.1.9 Read Track Command

3.5.1.9.1 Command Phase

Table 92. Read Track Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	MFM	0	0	0	0	1	0
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Track Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End-of-Track							
Byte 7	Gap Length							
Byte 8	Data Length							

3.5.1.9.2 Execution Phase

Data read from the disk drive is transferred to the system via DMA or non-DMA modes.

3.5.1.9.3 Result Phase

Table 93. Read Track Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Track Number
Byte 4	Head Address
Byte 5	Sector Number
Byte 6	Number of Data Bytes in Sector

3.5.1.10 Recalibrate Command

3.5.1.10.1 Command Phase

Table 94. Recalibrate Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	1

Table 94. Recalibrate Command Phase *(Continued)*

	7	6	5	4	3	2	1	0
Byte 1	0	0	0	0	0	0	US	US

3.5.1.10.2 Execution Phase

The disk drive head is stepped out to Track 0.

3.5.1.10.3 Result Phase

This command has no result phase.

3.5.1.11 Relative Seek Command

3.5.1.11.1 Command Phase

Table 95. Relative Seek Command Phase

	7	6	5	4	3	2	1	0
Byte 0	1	DIR	0	0	1	1	1	1
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Relative Cylinder Number							

3.5.1.11.2 Execution Phase

The disk drive head is stepped in or out a programmable number of tracks.

3.5.1.11.3 Result Phase

This command has no result phase.

3.5.1.12 Scan Equal Command

3.5.1.12.1 Command Phase

Table 96. Scan Equal Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MFM	SK	1	0	0	0	1
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Track Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End-of-Track							
Byte 7	Gap Length							
Byte 8	Scan Test							

3.5.1.12.2 Execution Phase

Data transferred from the system to the controller is compared to data read from the disk.

3.5.1.12.3 Result Phase

Table 97. Scan Equal Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Track Number
Byte 4	Head Address
Byte 5	Sector Number
Byte 6	Number of Data Bytes in Sector

3.5.1.13 Scan High or Equal Command

3.5.1.13.1 Command Phase

Table 98. Scan High or Equal Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MFM	SK	1	1	1	0	1
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Track Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End-of-Track							
Byte 7	Gap Length							
Byte 8	Scan Test							

3.5.1.13.2 Execution Phase

Data transferred from the systems to the controller is compared to data read from the disk.

3.5.1.13.3 Result Phase

Table 99. Scan High or Equal Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Track Number
Byte 4	Head Address
Byte 5	Sector Number